

Message Text

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PAGE 01 OECD P 08575 01 OF 02 071543Z

47

ACTION EB-07

INFO OCT-01 CIAE-00 COME-00 DODE-00 NSAE-00 TRSE-00 EUR-12

ERDA-05 ISO-00 MC-02 OES-03 /030 W

----- 023142

R 071537Z APR 75

FM USMISSION OECD PARIS

TO SECSTATE WASH DC 6377

C O N F I D E N T I A L SECTION 01 OF 02 OECD PARIS 08575

EXCON

E.O.11652: XGDS1

TAGS: ESTC, COCOM

SUBJECT: REVIEW OF IL 1565 - COMPUTERS

REF: A. STATE 32423

B. OECD PARIS 8404

1. ITALIAN DEL HAS PROPOSED FOLLOWING ADDITION TO NOTE
11 OF US REVISED PROPOSAL ON IL 1565:
ADD TO NOTE 11 THIS NEW PARAGRAPH, FOLLOWING PARAGRAPH
(D).

(C) THE DIGITAL COMPUTERS AND/OR DEVICES ARE LIMITED AS
FOLLOWS:

- (1) THE CPU NUMERICAL PROCESSING RATE DOES NOT
EXCEED 1 MILLION BITS PER SECOND, FOR UNITS
CAPABLE OF ARITHMETIC OPERATIONS.
- (2) THE CPU DATA HANDLING RATE DOES NOT EXCEED 2
MILLION BITS PER SECOND.
- (3) THE TOTAL INTERNAL MEMORY AVAILABLE TO THE USER
DOES NOT EXCEED 32768 BITS.
- (4) FOR PERIPHERAL DEVICES WITH WHICH THE COMPUTER
IS EQUIPPED:

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PAGE 02 OECD P 08575 01 OF 02 071543Z

(I) NO MORE THAN ONE MAGNETIC TAPE TRANSPORT;

(II) MAGNETIC TAPE TRANSPORTS WHICH DO NOT EXCEED:

- (A) 1600 BITS PER INCH PER TRACK;
- (B) 9 TRACKS PER 1/2 INCH (12.7 MM) TAPE WIDTH;
- (C) 1/2 INCH (12.7 MM) TAPE WIDTH; AND
- (D) 25 INCHES PER SECOND TAPE READ/WRITE SPEED.

(III) ADDITIONAL PERIPHERAL DEVICES

ARE RESTRICTED TO THE FOLLOWING TYPES:

- (A) PERIPHERAL DEVICES DEFINED UNDER NOTE 1 (WHICH ARE NOT EMBARGOED);
- (B) PERIPHERAL DEVICES DEFINED UNDER NOTE 6 (WHICH MAY BE SHIPPED UNDER ADMINISTRATIVE EXCEPTION PROCEDURE);
- (C) MAGNETIC CARD UNITS, BADGE AND TAG READERS AND OTHER DISCRETE MEDIA HANDLING UNITS.

DEFINITION OF TERMS USED IN NOTE 11:

(1) CPU NUMERICAL PROCESSING RATE IS DEFINED AS THE RATIO BETWEEN:

- THE NUMBER OF BITS USED TO REPRESENT AN ARITHMETIC OPERAND, AND;
- THE AVERAGE TIME REQUIRED FOR EXECUTION OF A MULTIPLICATION OPERATION;

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PAGE 01 OECD P 08575 02 OF 02 071547Z

47

ACTION EB-07

INFO OCT-01 CIAE-00 COME-00 DODE-00 NSAE-00 TRSE-00 EUR-12

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C O N F I D E N T I A L SECTION 02 OF 02 OECD PARIS 08575

EXCON

SAID RATIO BEING EVALUATED FOR THE MOST EFFICIENT ARITHMETIC DATA CODING AND MULTIPLICATION TECHNIQUE (CONTROLLED BY HARDWARE, FIRMWARE OR SOFTWARE) WHICH IS MADE AVAILABLE TO THE USER.

(2) THE CPU DATA HANDLING RATE IS DEFINED AS THE RATIO BETWEEN:
THE MAXIMUM NUMBER OF MEMORY BITS THAT CAN BE ACCESSED IN PARALLEL, AND:
-THE MINIMUM TIME REQUIRED FOR THE EXECUTION OF ANY INSTRUCTION INVOLVING ACCESS TO THE ABOVE DEFINED NUMBER OF BITS, LOCATED IN MEMORY.

(3) THE TOTAL INTERNAL MEMORY AVAILABLE TO THE USER IS EVALUATED INCLUDING ANY ALTERABLE INTERNAL STORAGE ELEMENT USED TO STORE DATA, FIRMWARE AND/OR SOFTWARE INSTRUCTIONS THAT MAY BE ALTERED BY THE USER.
USER-REPLACEABLE FIXED STORAGE ELEMENTS MUST BE TAKEN INTO ACCOUNT.

ACTION REQUESTED: URGENT REVIEW BY APPROPRIATE EXPERTS AND FORMULATION OF US POSITION ON ITALIAN PROPOSAL PRIOR TO APRIL 23.

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